

N-Channel MOSFET

General Description

The WSD40100DN56 is the highest performance trench N-Channel MOSFET with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The WSD40100DN56 meet the RoHS and Green Product requirement, 100% E_{AS} guaranteed with full function reliability approved.

Features

- 100% UIS + R_g Tested.
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

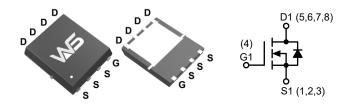
Product Summery

BV _{DSS}	R _{DS(ON)}	I _D
40V	2.0mΩ	100A

Applications

 Power Management for Industrial DC/DC Converters

DFN5X6-8L Pin Configuration



Absolute Maximum Ratings (T_A=25°C, Unless Otherwise Noted)

Symbol	Parameter		Rating	Units	
V _{DS}	Drain-Source Voltage		40	.,	
V _{GS}	Gate-Source Voltage		±20	V	
. 7		T _C =25°C	100		
I _D ⁷	Continuous Drain Current	T _C =100°C	75	A	
I _{DM} ³	Pulse Drain Current		300		
D 2	Power Dissipation	T _C =25°C	157	10/	
P _D ²		T _C =100°C	62	W	
I _{AS} ³	Single pulse Avalanche Current		47	А	
E _{AS} ³	Single pulse Avalanche Energy L=0.3mH		331	mJ	
T _{STG}	Storage Temperature Range		-55 to 150		
T _J	Operating Junction Temperature Range		-55 to 150	°C	
D 14	Thermal Resistance-Junction to Ambient	t≤10s	20		
$R_{\theta JA}^{1,4}$		Steady State	50	°C/W	
$R_{\theta JC}$	Thermal Resistance-Junction to Case		0.8		



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Electrical Characteristics (T_{.1}=25°C, Unless Otherwise Noted)

Symbol	Parameter	Conditions		Min.	Тур.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250μA		40			V
		V _{GS} =10V , I _D =20A			2.0	3.5	
R _{DS(ON)}	Static Drain-Source On-Resistance		T _J =125°C		3.25	4.0	mΩ
		V _{GS} =4.5V , I _D =20A			3.0	4.5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_{D}=250\mu A$		1.0	1.9	2.5	V
	Drain Source Loakage Current	V _{DS} =40V , V _{GS} =0V				1.0	
I _{DSS}	Drain-Source Leakage Current		T _J =55°C			5.0	μA
I _{GSS}	Gate-Source Leakage Current	V _{DS} =0V , V _{GS} =±20V	•			±100	nA
9 _{fs}	Forward Transconductance	V _{DS} =5V , I _D =20A			100		S
R_{G}	Gate Resistance	f=1.0MHz		1.0	2.0	3.1	Ω
Q_g	Total Gate Charge (10V)				68	95	
Q_g	Total Gate Charge (4.5V)	V _{DS} =20V , V _{GS} =10V	1 -204		28	40	
Q_{gs}	Gate-Source Charge	V _{DS} -20V, V _{GS} -10V	, I _D -20A		16.5		nC
Q_{gd}	Gate-Drain Charge				4.5		
Q _{oss}	Output Charge	V _{DS} =20V , V _{GS} =0V	V _{DS} =20V , V _{GS} =0V		37		
$T_{d(on)}$	Turn-On Delay Time				12.5		
T _r	Rise Time	V_{DS} =20V , V_{GS} =10V	' ,		9.5		no
$T_{d(off)}$	Turn-Off Delay Time	$R_L=1\Omega$, $R_{GEN}=3\Omega$			57.5		ns
T _f	Fall Time				10.5		
C _{iss}	Input Capacitance				5225		
C _{oss}	Output Capacitance	V_{DS} =20V , V_{GS} =0V ,	f=1.0MHz		895		pF
C _{rss}	Reverse Transfer Capacitance				200		

Diode Characteristics

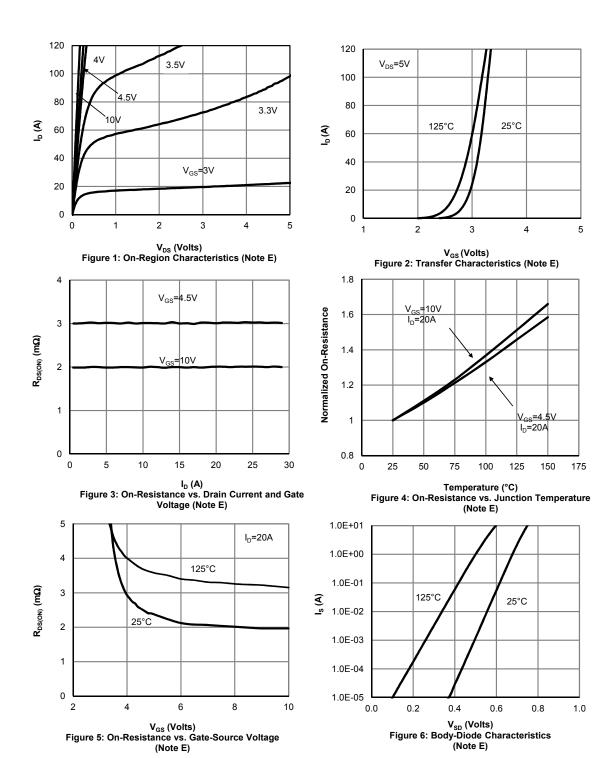
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
I _S ⁷	Continuous Source Current				100	Α
V _{SD}	Diode Forward Voltage	V _{GS} =0V , I _S =1A		0.7	1.0	V
t _{rr}	Reverse Recovery Time	l _E =20A , di/dt=500A/μs		20		ns
Q _{rr}	Reverse Recovery Charge	1 F-20A, αι/αι-300A/μ5		60		nC

Note:

- 1. The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- 3. Single pulse width limited by junction temperature $T_{J(MAX)}$ =150°C.
- 4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- 5. The static characteristics in Figures 1 to 6 are obtained using <300 μ s pulses, duty cycle 0.5% max.
- These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a
 maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.
- 7. The maximum current rating is package limited.
- 8. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.
- 9. The maximum current rating is silicon limited

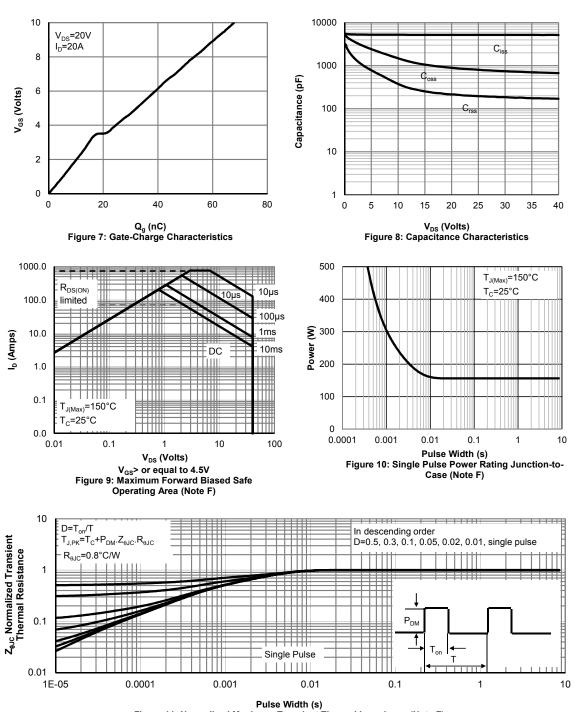


Typical Characteristics



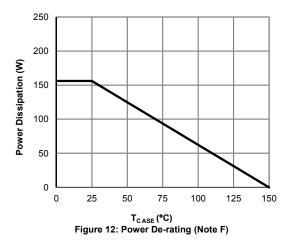


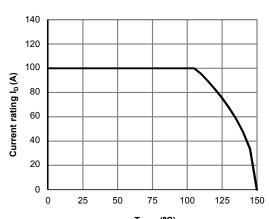
Typical Characteristics (Cont.)



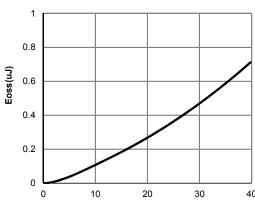


Typical Characteristics (Cont.)

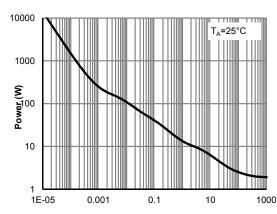




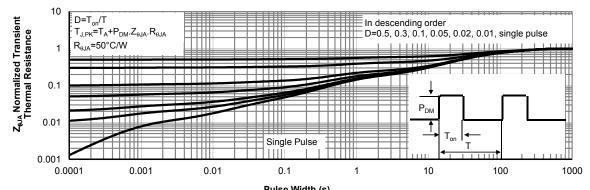
T_{C ASE} (°C)
Figure 13: Current De-rating (Note F)







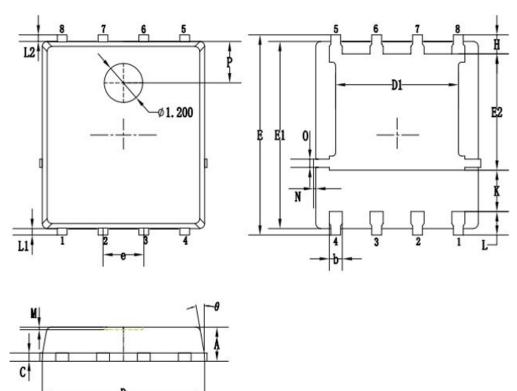
Pulse Width (s) Figure 15: Single Pulse Power Rating Junctionto-Ambient (Note H)



Pulse Width (s)
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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Packaging information



SYMBOLS	MILLIMETERS			
	MIN.	NOM.	MAX.	
А	0.90	1.05	1.20	
b	0.35	0.40	0.50	
С	0.20	0.25	0.35	
D	4.90	5.05	5.20	
D1	3.72	3.82	3.92	
Е	6.00	6.15	6.30	
E1	5.60	5.75	5.90	
E2	3.47	3.57	3.67	
е	1.27 BSC.			
Н	0.48	0.58	0.68	
K	1.17	1.27	1.37	
L	0.64	0.74	0.84	
L1/L2	0.20 REF.			
θ	8°	10°	12°	
М	0.08 REF.			
N	0	-	0.15	
0	0.25 REF.			
Р	1.28 REF.			



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